REMARKS:

Claims 1-25 are pending. Claims 1-25 are rejected.

Claim Rejections - 35 U.S.C. 102(E)

The Examiner has rejected claims 1-25 under 35 U.S.C. 102(e) as anticipated by Dacus et al. (U.S. Patent No. 6,008,698), herein Dacus. The Applicants include the following comments to clearly distinguish the claimed invention over the art cited by the Examiner, and respectfully request a favorable reconsideration of claims 1-25.

These rejections are respectfully disagreed with, and are traversed below.

The Examiner is respectfully reminded that for a rejection to be made under 35 U.S.C. 102(e), it is well recognized that "to constitute an anticipation, all material elements recited in a claim must be found in one unit of prior art", Ex Parte Gould, BPAI, 6 USPQ 2d, 1680, 1682 (1987), citing with approval In re Marshall, 578 F.2d 301, 304, 198 USPQ 344, 346 (CCPA 1978).

Regarding claim 1, which recites:

> "A power amplifier module operable over a range of output power levels, comprising an output transistor having an input coupled to an input node of the power amplifier module and an output coupled to an output node of the power amplifier module,
>
> the power amplifier module further comprising circuitry for **automatically compensating a load line of the output transistor for impedance variations** appearing at the output node,
>
> the circuitry comprising detection circuitry for generating a first detection signal having a value that is indicative of the **current flowing through the output transistor** and a second detection signal having a value that is indicative of the **voltage appearing <u>at the output</u> of the output transistor**, and
>
> further comprising compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, **and the current output power level** of the power amplifier module" (emphasis added).

The Examiner asserts that Dacus teaches:

> "power amplifier module operable over a range of output power levels, comprising:

an output transistor having an input coupled to an input node of the power amplifier module and an output coupled to an output node of the power amplifier module, the power amplifier module (col 1 lines 40-56) further comprising:

circuitry for automatically compensating a load line of the output transistor for impedance variations appearing at the output node (col 23 lines 5-60); and

a detection circuitry for generating a first detection signal having a value that is indicative of the current flowing through the output transistor and a second detection signal having a value that is indicative of the voltage appearing at the output of the output transistor (col 22 lines 62-67, col 24 lines 1-5), and further comprising:

compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, and the current output power level of the power amplifier module (col 23 lines 5-67, col 24 lines 1-30)" (emphasis added).

The Applicants respectfully assert that the Examiner has misinterpreted the teachings of Dacus. Consider the cited portions of Dacus:

"The dynamically adaptable supply current and voltage circuit 400 employs the **feedback control loop 78** of the dynamically adaptable supply current circuit 200 to vary the supply current, I_{SP} and I_{SF}, in the respective preceding gain stage 104 and final gain stage 106 of the RF amplifier 102.

The output terminal 317 of the variable power supply 302 is connected to the power terminal 110 of the final gain stage 106 of the RF amplifier 102 producing the supply current, I_{SF}, in the final gain stage 106, and the supply voltage, V_S, on the power terminal 110 of the final gain stage 106. The **input terminal 82 of the current detector 58 is connected to the output terminal 317 of the variable power supply 302**, and the **output terminal 83 of the current detector 58 is connected to the power terminal 108 of the preceding gain stage 104**, producing the supply current, I_{SP}, in the preceding gain stage 104 of the RF amplifier 102. The coupling terminal 84 of the current detector 58 is **connected to the first input terminal 85 of the signal processor 80**. The current detector 58 produces the sampled supply current signal, S_{ISP}, on the coupling terminal 84 of the current detector 58, influencing the supply current tracking signal, $S_{TRK-ISP}$, on the first input terminal 85 of the signal processor 80...

"The **signal processor 80** determines, scales, and integrates the difference between the control and envelope tracking signal, $S_{TRK-C-env1}$, and the supply current tracking signal, $S_{TRK-ISP}$, to produce a dynamic gate biasing signal, S_{DG1}, on the output terminal 87 of the signal processor 80. The output terminal 87 of the signal processor 80 is connected to the control terminal 112 of the RF amplifier 102, producing the dynamic gate biasing signal, S_{DG1}, on the control terminal 112 of the RF amplifier 102. The supply currents, I_{SP} and I_{SF},

are set to a desired level by the controller 402 and vary from that level with the output envelope signal, S_{env}" (col. 23, lines 6-59, emphasis added).

"The dynamically adaptable supply current and voltage circuit 400 also employs the variable power supply 302 and **feedback control loop 303** of the dynamically adaptable supply voltage circuit 300 to vary the supply voltage, V_S.

The **input terminal 313 of the voltage detector 304 is connected to the output terminal 317 of the variable power supply 302** and the output terminal 315 of the voltage detector 304 is connected to the second input terminal 309 of the signal processor 305. The voltage detector 304 produces the sampled supply voltage signal, S_{VS}, on the output terminal 315 of the voltage detector 304, influencing the supply voltage tracking signal, S_{TRK-VS}, on the second input terminal 309 of the signal processor 305" (col. 23, line 60 – col. 24, line 5, emphasis added).

"The signal processor 305 determines and scales the difference between the control and envelope tracking signal, $S_{TRK-C-env2}$, and the supply voltage tracking signal, S_{TRK-VS}, to produce a dynamic gate biasing signal, S_{DG2}, on the output terminal 311 of the signal processor 305. The output terminal 311 of the signal processor 305 is connected to the control terminal 310 of the variable power supply 302. The dynamic gate biasing signal, S_{DG2}, is produced on the control terminal 310 of the variable power supply 302. The supply voltage, V_S, is set to a desired level by the controller 402 and varies from that level with the output envelope signal, S_{env}" (col. 24, lines 17-29, emphasis added).

The cited portions of Dacus do not disclose or suggest "impedance variations appearing at the output node" as in claim 1. In fact, a word search of Dacus reveals no instances of the terms "impedance variations" or "impedance". Clearly, Dacus does not disclose or suggest "automatically compensating a load line of the output transistor for impedance variations appearing at the output node" as in claim 1.

The Examiner asserts the cited portions teach "a first detection signal having a value that is indicative of the current flowing through the output transistor". However, the cited portions of Dacus teach that the "current detector 58 produces the sampled supply current signal, S_{ISP}" based on "the supply current, I_{SP}, in the preceding gain stage 104 of the RF amplifier 102" and noting that "RF amplifier 102" produces "the supply current, I_{SF}, in the final gain stage 106". Clearly, "S_{ISP}" does not disclose or suggest "a value that is indicative of the current flowing through the output transistor". Rather, "S_{ISP}" appears to describe "the supply current,

I_{SP}, in **the preceding gain stage 104** of the RF amplifier 102". Thus, the cited portions of Dacus do not disclose or suggest "a first detection signal having a value that is indicative of the current flowing **through the output transistor**" as in claim 1.

The Examiner asserts the cited portions of Dacus teach "a second detection signal having a value that is indicative of the voltage appearing at the output of the output transistor". However, the cited portions of Dacus teach that the "input terminal 313 of the voltage detector 304 is connected to the output terminal 317 of the variable power supply 302". Clearly, the cited portions of Dacus do not disclose or suggest "a second detection signal having a value that is indicative of the voltage appearing at the **output** of the **output transistor**" as in claim 1.

Alternatively, the Examiner may be interpreting the "$S_{TRK\text{-}C\text{-}env1}$" and "$S_{TRK\text{-}C\text{-}env2}$" as the "first detection signal" and "second detection signal". If this is the case, then, clearly, Dacus does not disclose a separate signal indicative of "the current output power level of the power amplifier module". Thus, Dacus does not disclose or suggest "a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the **first and second detection signals, and** the **current output power level** of the power amplifier module" as in claim 1.

Dacus does not disclose or suggest "automatically compensating a load line of the output transistor for impedance variations", "a first detection signal having a value that is indicative of the current flowing through the output transistor", "a second detection signal having a value that is indicative of the voltage appearing at the output of the output transistor" and "a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, and the current output power level of the power amplifier module" as in claim 1. Thus, Dacus does not recite all material elements of claim 1. For at least this reason, claim 1 is in condition for allowance.

As claims 9, 17, 20 and 21 recite similar language to that discussed above with reference to claim 1, claims 9, 17, 20 and 21 are likewise in condition for allowance. As claims 2-8, 10-

16, 18-19 and 22-25 depend upon claims 1, 9, 17 and 21, they are likewise in condition for allowance. However, in order to fully address the Examiner's rejections regarding dependent claims 2-8, 10-16, 18-19 and 22-25, the Applicants submit the comments below.

Regarding claim 2, which recites:

> "A power amplifier module as in claim 1, further comprising an **impedance matching circuit** coupled **between the output of the output transistor and the output node**, the impedance matching circuit **presenting a variable impedance** that is controlled by an output signal from the compensation circuitry" (emphasis added).

The Examiner asserts that Dacus teaches this element at "col 9 lines 10-22". Consider the cited portions of Dacus:

> "As shown in FIG. 7, the **current detector 58** is a current mirror, which employs a PNP bipolar transistor Q1 and a diode D2 to **sample the supply current, I_{SP}**, entering the preceding gain stage 104 of the RF amplifier 102. The cathode of the diode D2 is connected to the base of the transistor Q1. The anode of the diode D2 is connected to the input terminal 82 of the current detector 58 through a resistor R10. The cathode of the diode D2 is connected to the output terminal 83 of the current detector. The emitter of the transistor Q1 is connected to the input terminal 82 of the current detector 58 through a resistor R11. The collector of the transistor Q1 is connected to the coupling terminal 84 of the current detector 58 through a resistor R12" (emphasis added).

As disclosed, the cited portions describe a "current detector 58". There is no disclosure or suggestion of the "current detector 58" "presenting a variable impedance". Rather, the "current detector 58" is disposed so as "to sample the supply current, I_{SP}, entering the preceding gain stage 104". Clearly, the "current detector 58" is not disclosed or suggested as being disposed "between the output of the output transistor and the output node". Thus, Dacus does not disclose or suggest claim 2.

Regarding claim 4, which recites:

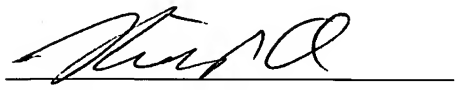
> "A power amplifier module as in claim 2, where the output signal from the compensation circuitry is generated when the current output power level **exceeds a predetermined output power level**" (emphasis added).

The Examiner asserts that Dacus teaches this element at "col 23 lines 5-67, col 24 lines 1-30". As disclosed in Dacus: the "signal processor 305 determines and scales the **difference** between the control and envelope tracking signal, $S_{TRK\text{-}C\text{-}env2}$, and the supply voltage tracking signal, $S_{TRK\text{-}VS}$, to produce a dynamic gate biasing signal, S_{DG2}" and "signal processor 80 determines, scales, and integrates the **difference** between the control and envelope tracking signal, $S_{TRK\text{-}C\text{-}env1}$, and the supply current tracking signal, $S_{TRK\text{-}ISP}$, to produce a dynamic gate biasing signal, S_{DG1}". There is no disclosure or suggestion of "a predetermined output power level" or that "the output signal from the compensation circuitry is generated when the current output power level **exceeds a predetermined output power level**" as in claim 4. Thus, Dacus does not disclose or suggest claim 4.

The Examiner is respectfully requested to reconsider and remove the rejection under 35 U.S.C. 102(e) based on Dacus, and to allow claims 1-25.

For the foregoing reasons, the Applicants believe that each and every issue raised by the Examiner has been adequately addressed and that this application is in a condition for allowance. As such, early and favorable action is respectfully solicited.

Respectfully submitted:



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